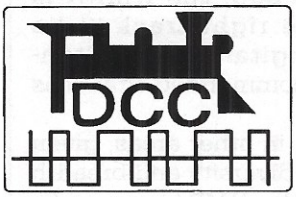
# Standards for Digital Command Control




**by: Stan Ames and Dave Cooper**

Over the past year the Electrical Committee has presented a series of Draft Standards and Recommended Practices for Digital Command Control. The NMRA Electrical Committee: Command Control Working Group is now pleased to present the completed standards for membership consideration.

**Why are these standards important?**

We are attempting to advance the hobby by providing a foundation for Digital Command Control (also called DCC). By establishing base level track electrical and communications protocols, the NMRA is defining compatibility for the next generation of train control. We believe that standards are essential in order to promote the development of this important segment of our hobby, and to provide for basic interchange of equipment. This is not to say that this is the only accepted method for train control. Many creative methods exist now and more will exist in the future that have nothing to do with Digital Command Control. The intent of these standards is to provide a precise definition of DCC so that manufacturers can develop compatible equipment which will facilitate basic interchange of equipment.

**What's new in these Versions?**

Many enhancements were made as a result of general membership review of the proposal and significant input from the manufacturers. In addition to a general reworking of the documents, and removing any possible dependency on any known patents, the standards were expanded to facilitate compatibility with a greater number of existing systems. This means that it will be easier to develop equipment that is backward compatible with existing systems. We have already demonstrated a possible upgrade package for existing CTC-based receivers which allows these receivers to work with the CTC family of Command Stations, Digital Command Control, and conventional 12 volt DC power. In addition, we have worked with several manufacturers to provide possible upgrades to their existing command stations that allow simultaneous control of existing products as well as new decoders which conform with the proposed digital standards.

**What does the Numbering Scheme signify?**

The technical department has devised a new numbering scheme by which similar standards are grouped together. The NMRA Digital Command Control Standards are extensions of the base electrical standards which are covered in S-9. The various Recommended Practices for Digital Command Control will be numbered RP-9.1.X for hardware related Recommended Practices, and RP-9.2.X for software or packet format Recommended Practices. This numbering scheme helps organize related items and facilitates communicate.

**Summary**

We would like to take this opportunity to thank all of you who wrote and provided us comments on the draft documents. The comments pointed up many potential shortcomings and have resulted in a superior set of standards to vote on. We would also like to extend our thanks to the various manufacturers who have worked as a team so that the standards we are now voting on are the best technically possible while at the same time allowing cost-effective products to be built..

On behalf of the over 60 members of the NMRA Electrical Committee: Command Control Working Group, who have invested many thousands of hours of work into this proposal, we solicit your support in approving these standards.

| NMRA STANDARD | |
|---|---|
| ELECTRICAL STANDARD FOR DIGITAL COMMAND CONTROL, ALL SCALES | |
| S-9.1 | Revised January 1994 |

Communication from a *Digital Command Station* to a *Digital Decoder* is accomplished by transmitting a series of bits that convey instructions. A bit is a signal which represents one of two conditions, which we will call "1" and "0". This portion of the standard covers the electrical characteristics of the digital command control signal that encodes these bits.

## A: Technique For Encoding Bits

The NMRA baseline digital command control signal consists of a stream of transitions between two equal voltage levels that have opposite polarity[1]. Alternate transitions separate one bit from the next. The remaining transitions divide each bit into a first part and a last part. *Digital Command Stations* shall encode bits within this digital command control stream of transitions by varying the duration of the parts of the bits, or frequency of the transitions.

In a "1" bit, the first and last part of a bit shall have the same duration, and that duration shall nominally be 58 microseconds[2], giving the bit a total duration of 116 microseconds. *Digital Command Station* components shall transmit "1" bits with the first and last parts each having a duration of between 55 and 61 microseconds. A *Digital Decoder* must accept bits whose first and last parts have a duration of between 52 and 64 microseconds, as a valid bit with the value of "1".

In a "0" bit, the duration of the first and last parts of each transition shall nominally be greater than or equal to 100 microseconds. To keep the DC component of the total signal at zero as with the "1" bits, the first and last part of the "0" bit are normally equal to one another. *Digital Command Station* components shall transmit "0" bits with each part of the bit having a duration of between 95 and 9900 microseconds with the total bit duration of the "0" bit not exceeding 12000 microseconds. A *Digital Decoder* must accept bits whose first or last parts have a duration of between 90 and 10000 microseconds as a valid bit with the value of "0". Figure 1 provides an example of bits encoded using this technique.

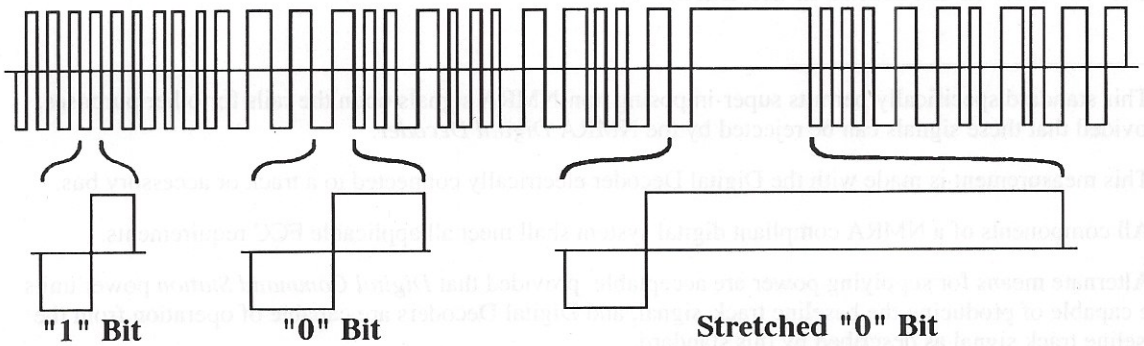



Figure 1: Bit Encoding

[1] Note that since a locomotive or piece of rolling stock can be placed upon a given section of track facing in either direction, it is impossible to define, from the point of view of a *Digital Decoder*, whether the first or last part of a bit will have the "positive" voltage polarity.

[2] All timing measurements are done between zero volt crossings.

## B: Command Control Signal Shape

The NMRA digital signal applied to the track by any *Digital Command Station* shall have the following characteristics, as measured under conditions ranging from no load to the maximum continuous load permitted by the power source. Transitions that cross the region between -4 volts and +4 volts shall occur at 2.5 volts per microsecond or faster. This signal may contain ripple at the zero-crossing transitions, provided that this ripple shall have a frequency of no less than 100 KHz and an amplitude of no greater than one fifth the total amplitude of the NMRA digital signal[3].

*Digital Decoders* shall be designed to correctly decode signals with transitions whose slope is 2.0 volts per microsecond or faster across the voltage range from -4 volts to +4 volts. A *Digital Decoder* shall correctly decode at least 95% of properly addressed baseline packets, as defined in S-9.2, in the presence of noise (and/or other types of signals) above 100 KHz with a total peak-to-peak amplitude of less than one fourth of the peak-to-peak amplitude of the NMRA digital signal[4].

The exact shape of the NMRA digital signal shall be designed to minimize electro-magnetic radiation such that a large layout operated using this standard can meet applicable United States Federal Communications Commission electro-magnetic interference requirements[5].

## C: Power Transmission and Voltage Limits For Transmitting Power Through the Rails

The baseline method for providing the power to operate locomotives and accessories, which shall be supported by all *Digital Command Stations* and *Digital Decoders,* is by full-wave rectification of the bi-polar NMRA digital signal within the *Digital Decoder*[6]. To facilitate this form of power transmission, bits must be sent continuously, in order to maintain power to the *Digital Decoders*. The RMS value of NMRA digital signal, measured at the track, shall not exceed by more than 2 volts[7] the voltage specified in standard S9 for the applicable scale[8]. In no case should the peak amplitude of the command control signal exceed +/- 22 volts. The minimum peak value of the NMRA digital signal needed to provide power to the decoder shall be +/-7 volts measured at the track. *Digital Decoders* intended for "N" and smaller scales shall be designed to withstand a DC voltage of at least 24 volts as measured at the track. *Digital Decoders* intended for scales larger than "N" shall be designed to withstand a DC voltage of at least 27 volts as measured at the track.

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[3] This standard specifically permits super-imposing non-NMRA signals upon the rails for other purposes, provided that these signals can be rejected by the NMRA *Digital Decoder.*

[4] This measurement is made with the Digital Decoder electrically connected to a track or accessory bus.

[5] All components of a NMRA compliant digital system shall meet all applicable FCC requirements.

[6] Alternate means for supplying power are acceptable, provided that *Digital Command Station* power units are capable of producing the baseline track signal, and Digital Decoders are capable of operation from the baseline track signal as described by this standard.

[7] The additional voltage is to compensate for voltage drop in the *Digital Decoder*, to ensure that the maximum voltage as specified in the NMRA Electrical Standard (S-9) is available at the motor brushes.

[8] Care should be taken to ensure that any motors exposed directly to the digital signal for extended periods have a stall rating that exceeds the amplitude of the signal, or sufficiently high impedance at 4-9 KHz to reduce the current to normal operating level. This appears to only be a concern for high-precision coreless can motors, which present a low impedance load, or for layouts using an NMRA digital signal with an amplitude in excess of +-18 volts

| NMRA STANDARD | |
|---|---|
| COMMUNICATIONS STANDARD FOR DIGITAL COMMAND CONTROL, ALL SCALES | |
| S-9.2 | Revised January 1994 |

This standard covers the format of the information sent via *Digital Command Stations* to *Digital Decoders*. A *Digital Command Station* transmits this information to *Digital Decoders* by sending a series of bits using the NMRA digital signal described in S-9.1. This sequence of bits, termed a packet, is used to encode one of a set of instructions that the *Digital Decoder* operates upon. Packets must be precisely defined to ensure that the intended instructions can be properly encoded and decoded.

## A. General Packet Format

The following sequence of bits defines a valid NMRA packet. Any sequence of bits not meeting the full specifications of this general packet format is not, for the purpose of this standard, a "packet". *Digital decoders* should not act on any instructions that are not contained within a valid packet while in the NMRA digital mode of operation[1]. Note, portions within square [ ] brackets must occur one or more times.

Preamble: The preamble to a packet consists of a sequence of a minimum of ten bits each of which has the value of "1".

Packet Start Bit: The packet start bit is the first bit with a value of "0" that follows a valid preamble. The Packet Start Bit terminates the preamble and indicates that the next bits are an address data byte.

Address Data Byte: The first data byte of the packet normally contains eight bits of address information[2]. The first transmitted address bit shall be defined to be the most significant bit of the address data byte. Address Data Bytes with values 00000000, 11111110, and 11111111 are reserved for special operations and must not be transmitted except as provided in this Standard or associated Recommended Practices.

[ Data Byte Start Bit: This bit precedes a data byte and has the value of "0".

Data Byte: Each data byte contains eight bits of information used for address, instruction, data, or error detection purposes. The first transmitted data bit of each data byte shall be defined to be the most significant bit of the data byte. ]

Packet End Bit: This bit marks the termination of the packet and has a value of "1"[3].

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[1] It is permissible for *Digital Decoders* to accept formats in addition to the NMRA General Packet Format. See Section C for details.

[2] The first byte can also be used in special cases to indicate instructions. See the Service Mode Recommended Practice (RP-9.2.3) for an example of this dual use.

[3] The Packet End Bit may count as one of the ten preamble bits of the subsequent packet if there are no inter-packet bits.

Figure 1 provides an example of an acceptable command control packet that uses three data bytes: one address data byte, one instruction data byte and one error detection data byte.

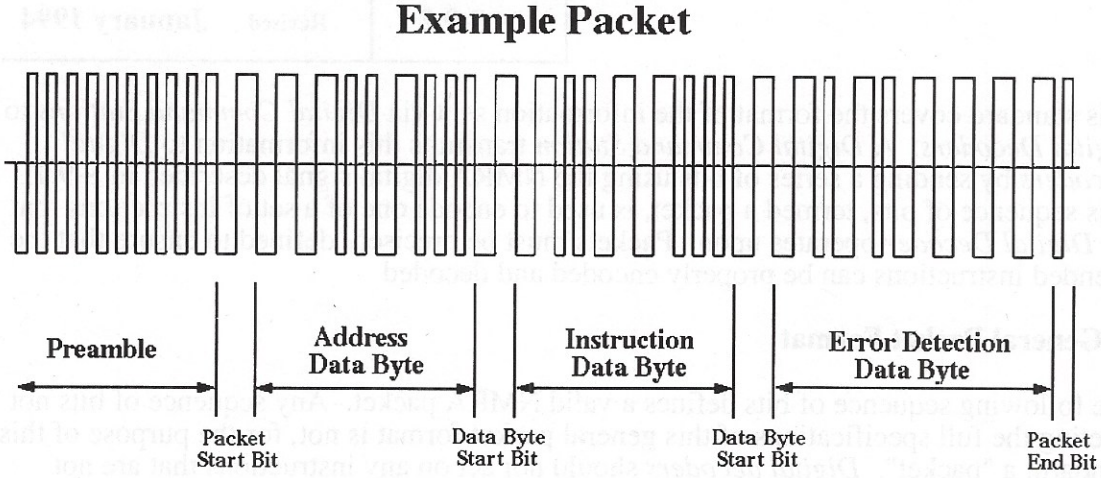


Figure 1 Example Packet Type

## B: Baseline Packets

The Baseline Packets are included to provide the minimum interoperability between different systems. More complex packet formats that support different types of decoders, additional functions, addresses and speeds are provided in the Extended Packet Format Recommended Practice (RP-9.2.1). It is the intention of this Standard that, in order to conform: a *Command Station* must encode operator control input in conformance with the Baseline Packet semantics; and a *Digital Decoder* must recognize and provide suitable locomotive control electrical output in conformance with the Baseline Packet semantics.

### Speed and Direction Packet For Locomotive Decoders

1111111111 0 0AAAAAAA 0 01DUSSSS 0 EEEEEEEE 1
Byte One Byte Two Byte Three

Byte One: Address Data Byte = 0AAAAAAA The address data byte contains the address of the intended recipient of the packet. Every *Digital Decoder* shall be capable of retaining and recognizing its own address for purposes of responding to Baseline Packets. Locomotive *Digital Decoders* shall support the full range of baseline addresses in such a manner that this address is easily configurable by the user[4]. It is acceptable for *Digital Command Stations* to restrict the number of valid addresses supported so long as this restriction is clearly and plainly labeled on the package and in the instructions.

[4] The Service Mode Recommended Practice (RP-9.2.3) contains one example of an acceptable method for user address configuration.

Byte Two: Instruction Data Byte = 01DUSSSS The instruction data byte is a data byte used to transmit speed and direction information to the locomotive *Digital Decoder*. Bits 0-3[5] provides 4 bits for speed (S) with bit 0 being the least significant speed bit. Bit four of the packet (U) can have a value of "1" or "0" and is not defined by the baseline[6]. Bit 5 provides one bit for direction (D). When the direction bit (D) has a value of "1" the locomotive should move in the forward direction[7]. A direction bit with the value of "0" should cause the locomotive to go in the reverse direction. Bits 7 and 6 contain the bit sequence "01"[8] which are used to indicate that this instruction data byte is for speed and direction.

| | Data Byte Bits 3-0 | | | Speed Step | | | |
|---|---|---|---|---|---|---|---|
| 0000 | Stop | 0100 | Step 3 | 1000 | Step 7 | 1100 | Step 11 |
| 0001 | EStop* | 0101 | Step 4 | 1001 | Step 8 | 1101 | Step 12 |
| 0010 | Step 1 | 0110 | Step 5 | 1010 | Step 9 | 1110 | Step 13 |
| 0011 | Step 2 | 0111 | Step 6 | 1011 | Step 10 | 1111 | Step 14 |

* Digital Decoders should bring locomotive to an immediate stop as quickly as possible

Figure 2 Speed Table for Baseline Packet

Byte Three: Error Detection Data Byte = EEEEEEEE The error detection data byte is a data byte used to detect the presence of transmission errors. The contents of the Error Detection Data Byte shall be the bitwise exclusive OR of the contents of the Address Data Byte and the Instruction Data Byte in the packet concerned. (e.g. the exclusive OR of bit 0 of the address data byte and bit 0 of the instruction data byte will be placed in bit 0 of the error detection data byte...) *Digital Decoders* receiving a Baseline Packet shall compare the received error detection data byte with the bitwise exclusive OR of the received address and instruction data bytes and ignore the contents of the packet if this comparison is not identical.

The example packet shown in figure 1 illustrates a baseline packet with the instruction to locomotive 55 to proceed in the forward direction at speed step 6.

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[5] Bits within a byte are numbered right to left with bit 0 (the right most bit) being the least significant bit and bit 7 (the left most bit) being the most significant bit.

[6] The Extended Packet Format Recommended Practice (RP-9.2.1) contains the preferred use of this bit.

[7] Forward in this case is in the direction of the front of the locomotive, as observed from the engineer's position within the locomotive.

[8] Other bit patterns in bits 7 and 6 are reserved for other types of instruction data, and are defined in the Extended Packet Format Recommended Practice (RP-9.2.1).

**Digital Decoder Reset Packet For All Decoders**

1111111111 0 00000000 0 00000000 0 00000000 1
Byte One Byte Two Byte Three

A three byte packet, where all eight bits within each of the three bytes contains the value of "0", is defined as a Digital Decoder Reset Packet. When a *Digital Decoder* receives a Digital Decoder Reset Packet, it shall erase all volatile memory (including any speed and direction data), and return to its normal power-up state. If the *Digital Decoder* is operating a locomotive at a non-zero speed when it receives a Digital Decoder Reset, it shall bring the locomotive to an immediate stop.

Following a Digital Decoder Reset Packet, a *Command Station* shall not send any packets with an address data byte between the range "01100100" and "01111111" inclusive within 20 milliseconds, unless it is the intent to enter service mode[9].

**Digital Decoder Idle Packet For All Decoders**

1111111111 0 11111111 0 00000000 0 11111111 1
Byte One Byte Two Byte Three

A three byte packet, whose first byte contains eight "1"s, whose second byte contains eight "0"s and whose third and final byte contains eight "1"s, is defined as a Digital Decoder Idle Packet. Upon receiving this packet, *Digital Decoders* shall perform no new action, but shall act upon this packet as if it were a normal digital packet addressed to some other decoder.

## C: Frequency Of Packet Transmission

Packets sent to *Digital Decoders* should be repeated as frequently as possible, as a packet may have been lost due to noise or poor electrical conductivity between wheels and rails. A *Digital Decoder* shall be able to act upon multiple packets addressed to it, provided the time between the packet end bit of the first packet and the packet start bit of the second packet are separated by at least 5 milliseconds[10]. Manufacturers of decoders are encouraged to provide automatic conversion for a variety of power signals and command control formats in addition to the NMRA digital signal, provided that automatic conversion to these alternate power signals can be disabled. If automatic conversion is enabled, *Digital Decoders* must remain in digital mode and not convert to using any alternate power signal so long as the time between Packet Start Bits is less than or equal to 30 milliseconds in duration. If automatic conversion is disabled, *Digital Decoders* must remain in digital mode regardless of the timing of Packet Start Bits. It shall be possible to configure *Digital Command Stations* to transmit packets more frequently than once every 30 milliseconds as measured from the time between packet start bits[11].

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[9] *Digital Decoders* can have their configurations altered immediately after a digital decoder reset packet. See the Service Mode Recommended Practice(RP-9.2.3) for details.

[10] Care must be taken to ensure that two packets with identical addresses are not are not transmitted within 5 milliseconds of each other for addresses in the range between 112-127 as older decoders may interpret these packets as service mode packets (see RP-9.2.3).

[11] Some DCC decoders manufactured prior to the NMRA standards require a valid baseline packet be received every 30 milliseconds to prevent analog power conversion.